TOTAL ENGINEERING SERVICES TEAM, INC.
(TEST Inc.)

SCADAWARE®

PC BASED GIO
GENERIC INPUT/OUTPUT
INTERFACE

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INTRODUCTION

SCADAWARE supports the use of generic PC based industrial interfaces based on a product line originally designed by MetraByte Corporation. These interfaces have become a de-facto standard in the industry, and are available from other companies such as Action Instruments, Computer Boards Inc., and National Instruments. These boards are essentially generic in design, leading TEST to refer to this method of interface as GENERIC I/O, or GIO for short.

The actual circuit board used in the TEST SCADA system does not matter as long as the interface to the PC bus matches that of the original MetraByte design. In some cases, several equivalent Metrabyte boards are found in a single board from other manufacturers. In this case, the software system will treat the single board as if it were several separate boards.

The standard board uses by TEST in the Type 1200 RTU is a Computer Boards Model CIO-AD08. This product combines the functions of two MetraByte boards, the DAS-08 Analog to Digital Converter and the PIO-12 Parallel Digital interface. This document will reference the Computer Boards Inc. product, although any other compatible interface should work as shown. Note that the Computer Boards card is modified by TEST to include 3 counter channels rather than 2 as is found in the typical generic board.

GENERIC I/O SYSTEM DESIGN

Each group of I/O points defined for a generic I/O system permits the physical connection of some number of status inputs, status outputs, analog inputs, and counter (pulse)inputs. Each channel type is assumed to be interfaced through a number of standard interface circuits as defined by the original MetraByte product. Each interface can support a fixed number of points. However, the software allows for several boards to be installed permitting a very large number of total points to be accommodated in a single system.

The status (digital) inputs and outputs are assumed to be interfaced through a standard Intel 8255 Parallel Interface component. The actual circuitry on the board may be a different component as long as it emulates the functions of the 8255.

Analog inputs are interfaced with the DAS-8 A/D system which provides 8 multiplexed 0-5VDC

inputs. A single A/D converter on the board reads signals through the on-board multiplexer to select one of eight inputs for conversion. The circuit also provides select lines used to control external multiplexers, permitting analog input expansion up to 64 (8x8) points on a single DAS-8 interface circuit.

High speed counter inputs are handled by the Intel 8254 Counter/Timer chip. These devices provide 3 independent 16 bit counters per chip, and they may be on separate boards or combined with other circuitry. The original Metrabyte DAS-8 contained a single Intel 8254 counter chip with one of the channels dedicated to the A/D conversion circuitry. This provided 2 available counter channels. Later versions of this circuit (by other manufacturers) have eliminated the need for the dedicated channel, and may have made the counter channel available for external use. TEST modifies the standard Computer Boards CIO-AD08 so that is has 3 counter channels available per board. Additional counter chip boards can also be used to provide more than 3 counter inputs without the higher cost of the full CIO-AD08 interface card.

GENERIC I/O (GIO) DRIVER PROGRAM

The Generic I/O hardware provides conversion of physical inputs into computer compatible numbers (bits for status, and integers for analog). In order for the computer to process the numbers, a "driver" program translates them into a format useful to SCADAWARE. This driver is a built-in feature of SCADAWARE, eliminating the use of stand-alone software drivers which may be provided by the various hardware vendors.

The GIO driver takes care of scanning all input and output types, and placing the values in the proper position in the RTU's data table. From this point, SCADAWARE processes the information without regard to where it came from. Therefore, the driver only performs low-level operations for input and output. All high level functions such as engineering units conversion, alarm checks, etc. are done in the main program no matter where the data came from.

The driver works at two different levels. The first level is that of a "fast" program that scans quick moving channels like status inputs. This portion of the driver runs at each system tick, which is approximately every 50 milliseconds. Although the driver may deliver the information at this speed, other factors within SCADAWARE determine how often the data is processed at a higher level.

The other portion of the driver works as a regularly scheduled SCADAWARE task. This section operates the slower channels like analog inputs, including any AFD (analog for digital) points. The timing of this portion can be controlled just like any other task to help balance the CPU workload.

The driver program needs to know the address for each group of generic interface circuits, how many points that group has, and where the data will "map"into the local TSP data table. Each channel type (input, output, analog, counter) is treated as a separate unit, even if they reside on the same physical circuit card. Each driver group can handle several groups of each channel type, all of which must exist in an orderly fashion on the PC bus.

The PC base address for each interface type (input, output, analog, counter) determines the starting point of each point type. This starting (or base) PC address is provided to SCADAWARE as a parameter in the GIO configuration file. It tells the system where to find the standard GIO devices on the PC address bus. In the case of multiple circuits, the driver must be programmed with the proper "offset" in the PC address space at which each subsequent board is located.

The driver must also be told the number of physical points to scan for each point type. Points are assumed to be addressed sequentially on the interface card, and to map sequentially into the TSP data table. The interface points always begin at the first point on each circuit card. However, the destination points in the TSP table do not have to begin with one, although this is almost always the case.

PC ADDRESS OFFSETS

The GIO design provides for a specific number of points on each type; 64 for analog, 24 for status, and 3 for counter. If the driver is programmed to deal with more than these limits, it automatically assumes that more than one board is present, and determines the addresses for each board using the offset value mentioned above. The standard offset is 16 (hex $10), although it may be different on some cards.

Therefore, programming the driver for 32 status points automatically sets up the system for 24 points in the first circuit, and 8 in the next. The address of the first circuit is specified by the user in the configuration file. The address of the second circuit is determined automatically by adding the offset to the first board's address. If the first status circuit begins at $320, and the offset is $10, then SCADAWARE will look for the second circuit at $330.

TSP DATA TABLE LOCATIONS

Physical points interfaced to the PC bus hardware are mapped into corresponding locations in the TSP data table. This mapping is done with starting points and counts. The driver is told where to put the first point, and how many to scan. The one-to-one relationship of physical points to TSP data table points is calculated automatically from the starting point and count provided by the user.

In most cases, the first points on the interface will correspond to the first points of the TSP data table. Thus, physical analog input number 1 will map to A1, the second to A2, and so on. This is also true for status inputs, status outputs, and counters. The only variation from this one-to-one scheme is when AFD (analog for digital) points are processed. The AFD points will interrupt the normal one-to-one relationship between physical analogs and TSP analogs. The gap is exactly equal to the number of AFD points which were relocated from the analog scan to the status input scan. This is further explained in another section.

STATUS INPUTS

Normal status inputs are interfaced through one or more Intel 8255 compatible parallel interface circuits. Each 8255 provides three 8 point groups, which can be configured for either input or output. The TEST system assumes that these ports will be assigned sequential PC bus addresses, and that the status input points will be installed before the output points. Also, each group of 8 bit points must be all input or output. A single 8 bit status group cannot contain mixed I/O.

These physical status inputs must be mapped into corresponding status inputs in the TSP data table. Normally, all 8 points per port address are used in the RTU data table, although this is not specifically required. Therefore, it is possible to set up a GIO system which uses only the first 4 inputs, or the first 12, if that is all that is required for a specific application. However, the left over bits will not be accessible for any other purpose.

Specification of a status input group will consist of a configuration line with the following items:

1. Keyword "Status"
2. First chip base address in the PC I/O Space
3. Address Offset between sequential circuits
4. Number of Status input points (default is 16)
5. Location in the TSP data table (default is S1 of the first RTU in the DAT file)

```
                  1    2    3  4  5
EXAMPLE:       Status $328,16
               Status $328,32,12, 1 ; use only 12 points
               Status $328,16,14, S4 ; use other than S1 as start of map
```

STATUS OUTPUTS

Output points are very similar to status points, with one bit per I/O point and 8 bits per PC bus port address. Status inputs and outputs are interfaced using the same Intel 8255 circuit. However, each group of 8 points on that circuit must be either input or output. Because the I/O can share a common 8255 circuit, specification of outputs must be made with consideration to how many status input groups will also be tied into the same 24 point interface.

Each 8255 has 3 ports, referred to as A, B, and C. Each port can be programmed as either input or output. To reduce complexity, the strategy used by the SCADAWARE GIO system requires that status inputs be addressed first, in 8 point groups, followed by outputs, also in 8 point groups. Note that it is possible to leave a gap between the two. This might be desirable to allow room for expansion of the status inputs at a later date.

For purposes of the output driver, the base address of the system is the base address of the first 8255 used for outputs. Any 8255 circuits in a sequence that are used exclusively for status inputs are not considered in the output setup. Only the first output circuit, which may include some prior status inputs, is used to specify the base address of the output system.

In a small system (24 total status I/O), the base address of the output 8255 will be the same as the input circuit. On a larger system, with multiple 8255 interfaces, the base address specified to the output driver will be higher than that specified for status inputs. The difference will be the board offset value (normally 16, or hex $10), times the number of boards. If the outputs are on the second 8255 board, and the first board was at $320, then the output base will be $330. If there are three 8255 boards, and the first output is on the third one, then the base for the output will be $340.

Because status inputs may be on the same chip as outputs, an additional parameter must be provided to the output driver. This parameter, called the "chip offset," tells the driver how many 8 bit status input groups are also on the first output chip. This value can be 0, 1, or 2. Note that it cannot be 3, because that would mean that the entire chip was used for status inputs, leaving no room for outputs.

Example: Remember that the chip has 3 ports. If the entire chip (ports A-B-C) is used for outputs, then the offset is 0. However, if the first 2 ports (A-B) are used for status input, then the driver will be programmed to offset 2 ports (from the chip's base address) when starting the output scan.

Specification of a status output group will consist of a line with the following items:

1. Keyword "OUTPUT"
2. Address First chip base address in the PC I/O Space
3. Address Offset between sequential circuits
4. Number of Status output points (default is 8)
5. Location in the RTU I/O Table (default is 1)
6. Chip offset for first output port (default is 2)

```
EXAMPLE:
Output $328, 8, 16, 1, 2; 8 outputs on port C of chip at $328. Status is ports A and B
Output $328, 4, 16, 04.1 ;4 outputs mapped starting with Output channel 4
```

ANALOG INPUTS

The analog input circuitry is based on the MetraByte DAS-8 multiplexed A/D converter card. This design uses a single 12 bit, bipolar A/D converter connected to an on-board 8 point multiplexer device. This accommodates 8 separate single ended analog signals by a single A/D converter circuit. The computer can access the 8 inputs, one at a time, by selection of the proper channel on the on-board multiplexer. On a TEST RTU, these points are normally connected via CAT (Counter Analog Termination) cards, which also happen to interface the high-speed counter circuits described elsewhere.

SCADAWARE permits each of the 8 on-board analog inputs can be further expanded with external analog multiplexers, normally located on MAT (Multiplexed Analog Termination) cards. With

this scheme, each of the original 8 standard analog inputs are multiplexed into 8 new analogs, giving a total of 8*8=64 total analog inputs per DAS-8 board. Note that the external multiplexer does not provide 8 *additional* inputs. Rather, it converts a single input into 8, with a net gain of 7 points.

Both externally multiplexed and normal DAS-8 analog points can be mixed in the same system. The externally multiplexed points come first, in groups of 8, followed by the remaining non-multiplexed points.

IMPORTANT: Each group of 8 Multiplexed points causes the loss of one non-mpx point, for a net gain of 7. Adding a MAT card does not add 8 inputs. It adds only 7, because although 8 MPX points are indeed added, one non-mpx is lost for use as a multiplex input. The table below details how many total points will actually be available for various input point ranges.

ANALOG POINTS	MAT MPX POINTS	CAT POINTS	MATB DS	MPX CARD POINTS	CAT CARD POINTS	
1-8	0	8	0	***	A1-A8	
9-15	8	7	1	A1-A8	A9-A15	
16-22	16	6	2	A1-A16	A17-A22	
23-29	24	5	3	A1-A24	A25-A29	
30-36	32	4	4	A1-A32	A33-A36	
36-43	40	3	5	A1-A40	A41-A43	
44-50	48	2	6	A1-A48	A49-A50	
51-55	56	1	7	A1-A56	A57	
57-64	64	0	8	A1-A64	***	

The arrangement of mpx and non-mpx points is made automatically by SCADAWARE based on the total Analog Inputs specified in the GIO configuration file. Note that the number of available points may be higher than that requested because of the tradeoff in mpx and non-mpx points. However, SCADAWARE will always make available at least the number which was specified. The driver will always place the multiplexers in the first channels, and will use non external multiplexer channels at the end. Any unused points will simply be ignored.

As a simple example, consider a system which requires 29 analog points. This would be done with three external multiplexers (for a total of 24 points) followed by 5 direct analog inputs. The 5 points were left over from the original 8 that the DAS-8 interface can directly handle. The first 3 DAS-8 analogs were used for the external multiplexers, leaving 5 direct DAS-8 points still available. Normally, these left-over direct inputs are interfaced with a TEST CAT termination board that also provides access to the counter input channels.

MULTIPLE ANALOG BOARDS

If more than 64 total points are specified for one group, the system will assume multiple sequential DAS-8 interfaces, each separated by an offset on the PC bus. Multiplexed analog input cards will handle the first points in a modulo 64 manner, with the final group following the scheme of the above table.

For a larger example, consider if a total of 96 analogs were specified. Because each DAS-8 can handle only 64 points, two boards will be required. The system will assign the first 64 analogs to the first board, all handled by 8 point multiplex cards. The remaining 32 will be handled according to the above table as if 32 were specified: 4 MPX cards will be used, providing 32 points, with room for another 4 non-mpx points. So specifying 96 points actually sets up the system for:

First DAS-8 board 64 points = 8 MAT Cards, with analogs A1-A64, no CAT card
Second board 36 points = 4 Mat cards (A65-96), 1 CAT (A97-A100)

ANALOG POINT PROGRAMMING

Specification of an analog input group will consist of a line with the following items:

1. Keyword "AIN" or "ANALOG"
2. PC bus address. First circuit base address in the PC I/O Space
3. Number of analog input points to scan (default is 8)
4. Board Offset between sequential circuits
5. Location in the SCADAWARE TSP I/O Table (default is A1)
6. Analog For Digital Block size
7. First AFD status channel

```
EXAMPLE:
Ain, $330,22,16,1 ; 22 points with 2 MAT and 1 CAT board
Ain $320, 15      ; 15 default points with 1 MAT and 1 CAT
```

ANALOG CONVERSION PARAMETERS

The analog conversion process is relatively slow compared to other computer operations. The SCADAWARE driver has several settings which optimize the performance of the A/D subsystem for each particular CPU configuration. These settings are set automatically when the driver first starts, but can be overridden with special entries in the GIO file. The parameters for the analog system are:

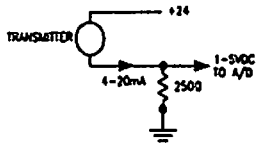
Wait Determines how long the system will wait for an analog conversion before signaling an error with the Alert channel. Typical values range from 10 to 200.
MIN Determines minimum change in the raw analog value which requires notification of SCADAWARE. Setting this value higher reduces flickering of jittery analog points.
DELAY Determines the loop count used by the driver to allow settling of analog multiplexers. Typical values are from 3 to 50.

Setting these parameters is explained in the section on GIO Driver Setup.

ANALOG INTERFACE HARDWARE

The analog circuitry is bipolar in that it accepts negative as well as positive voltages, always measured to system ground. The actual A/D converter measures +-5 VDC, and no pre-amp is normally provided on these cards. This means that the actual field voltage input to the card (or to an external multiplexer) must be between -5 and +5 VDC. TEST's MAT and CAT termination cards provide the necessary hardware to convert standard instrumentation signals (such as 4-20ma) into what is required by the A/D converter.

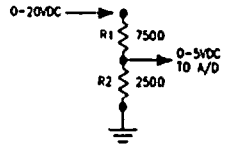
For example, if 4-20ma loop signals are to be sensed, a resistor is necessary to generate the voltage actually read by the A/D converter. This field voltage, at full scale of 20ma, is equal to the loop resistor ohms * .020 amp. So, if a 250 ohm resistor is used, a voltage of 5 volts will be generated at full scale.



ANALOG CURRENT SENSING

If a field voltage higher than 5VDC is to be measured, then a voltage divider must be set up to lower the measured signal to 5 volts or less. This can be easily done on the TEST MAT or CAT termination boards, or it can be done on external terminal strips. For example if a 12V battery is to be monitored, it would be necessary to provide scaling resistors so that the maximum voltage at the A/D board is 5 volts. A maximum full scale must be selected that is larger than 12VDC to allow for charging

voltages, and a value of 20 Volts is normally used. This would require a voltage divider that breaks up the maximum 20 volt signal into 15 volt and a 5 volt segments, with the 5 volt segment being across the input to theA/D converter. The scheme is as follows:



ANALOG VOLTAGE SENSING

The input impedance of the analog card is > 15 Meg ohms, so the circuit loading by the card is minimal as long as relatively small values for R1 and R2 are used. Higher values limit the current drain on the sensed voltage supply. So, assume we want to limit the current to less than 20ma. The sum of R1+R2 would be determined by E=I*R to be 20/.020 = 1000 ohms. The voltage divider formula would then be used to determine the values of R1 and R2 as follows:

R2 = 250 Ohms, so R1 = 1000-250 = 750 Ohms. The calculation required for monitoring a 24 VDC input would be similar but would be based on a max voltage of 30VDC instead of 20VDC:

The A/D converter takes the analog input signal and generates a binary number that represents the position of the input signal over the full 12 bit scale. The raw data from the A/D converter would look as follows:

```
      MSB   7  6  5  4  3  2  1  0  LSB   7  6  5  4  3  2  1  0
12 bit Mode S  10 9  8  7  6  5  4        3  2  1  0  -  -  -  -
```

	CPU USES 2'S COMPLEMENTARY	HEX		A/D CONVERTER STRAIGHT BINARY	HEX
-32768	1000 0000 0000 0000	8000	-FS	0000 0000 0000	0000
-1	1111 1111 1111 1111	FFFF		0111 1111 1111	07FF
0	0000 0000 0000 0000	0000	Mid	1000 0000 0000	0800
+1	0000 0000 0000 0001	0001		1000 0000 0001	0801
+32767	0111 1111 1111 1111	7FFF	+FS	1111 1111 1111	0FFF

SCADAWARE uses a signed 16 bit integer system regardless of the actual precision of the A/D hardware. This is done so that other hardware drivers up to 16 bits can be accommodated in the future. The conversion for the DAS-8 interface involves shifting the 12 bits left 4 bits, and then subtracting $8000 to account for the input offset. The result is a standard 16 bit signed integer, with minus full scale = -32K, 0 = 0, and plus full scale = +32K. The raw converted integer value is placed in the TSP channel object by the driver. All further processing (engineering units and alarm checks) takes place in SCADAWARE and does not involve the driver itself.

ANALOG INPUT CALIBRATION

Each Analog Input card has a single A/D converter that is shared by all inputs, so calibrating a single point will set the calibration for all others. Adjustments on the card will vary, but generally consist of zero and span pots only. SCADAWARE's **CAL command** can be used to rapidly display a single analog input during calibration. Be sure the channel is set to allow negative numbers during the calibration process.

Start calibration by removing the channel's normal input source and then shorting the input to analog ground. Then adjust the ZERO pot until the channel reads 0 on any SCADAWARE display, preferably with the CAL command. Then place a full scale voltage (5 volt) on the input and set the SPAN pot until the channel reads full scale (value depends on the channel programming). There is typically some interaction between the zero and span, so repeat the process several times until the best values can be obtained.

AFD - ANALOG FOR DIGITAL INPUTS

AFD input points are analog inputs which are re-mapped by the driver into the TSP status input data table. AFD is a cost and space saving innovation designed by TEST for RTU's with many unused analog inputs. Although each GIO interface board can handle 64 analogs, the status I/O is limited to 24 points per board. Many systems use far fewer than 64 analogs, but more than 24 status inputs.

The AFD system permits the unused analog inputs to be re-mapped into status inputs, thereby increasing the available status inputs without additional traditional status input circuits. The tradeoff is processing speed because the analog inputs are scanned much slower than real status inputs. The speed is still adequate for most RTU applications, where detecting a closed switch in a second (rather than 50 ms) is still plenty fast enough. Important: *A point used for AFD cannot also be used as an analog.*

The re-mapped analog point is effectively reduced to 1 bit precision, where anything below half-scale is considered a 1, and above half-scale is a 0. The reverse logic is used to let the AFD points work similar to normal status inputs. Grounding a status or AFD inputs results in a logical "ON" setting.

The important terms for AFD are:

AFD	Analog for Digital. Using analog inputs for digital input purposes
AFD Block	How many points AFD will use within the physical analog scan table
Analog Group	How many analog points will be physically scanned by the driver
AFD Group	How many physical analogs will be used for status purposes
Physical Point	A termination point on any analog or AFD termination board
Logical Point	The resulting use of a physical point, either as a logical analog, or as a logical status.

Each analog driver group can have a single AFD block embedded within it. The block will typically allocate points in multiples of 8, although this is not a requirement. The AFD block will be treated as a sub-unit of the entire Analog Group, reducing the number of logical analogs by the specified amount. So a total analog group of 48 points which contains a 16 point AFD block will result in only 32 logical analogs for use in the TSP data table. Although 48 points will be scanned, 16 of them will be redirected to the status input table.

The GIO configuration file for this setup might be:

```
AIN $328 48 16 A1 16 A17 S9 ; block out 16 analogs for use in AFD at S9-24
                            ; Usable analogs reduced to 32
```

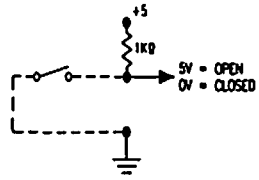
1. Keyword "AIN" or "ANALOG"
2. PC bus address. First circuit base address in the PC I/O Space
3. Number of analog input points to scan (default is 8)
4. Board Offset between sequential circuits
5. Location in the SCADAWARE TSP I/O Table (default is A1)
6. Analog For Digital Block size
7. First physical analog to remap into AFD
8. First AFD status channel (with optional range to specify AFD group size less than block size)

Note that setup of the analog driver with AFD is similar to a normal Analog driver. The addresses, total number of scanned points, and other parameters are entered on the normal AIN control line of the GIO file. Three additional parameters instruct the driver to divert a group of the analogs, beginning at a specified physical analog input, into the status input table.

The size of the AFD block determines how many analog points will be deleted from the TSP analog map. Normally, all of these AFD points will be directed to corresponding status input points. However, it is possible to block out more points than will be required. This option is necessary to permit a group of AFD points to reside in the middle of an analog group, rather than only at the end. Doing so permits a mix of Multiplexed Analogs, AFD points, and Non-Multiplexed (CAT terminations) to be made in a single circuit.

AFD points can be physically connected to any type of analog input termination. They can also

be connected to special AFD termination points which replace the normal analog scaling resistors with opto-isolated inputs. The driver cannot tell the difference. It will sample the analog input just as if it were a normal input. The only difference is that instead of placing the raw analog value into a TSP analog input channel, the driver makes the OFF/ON decision based on half-scale, and sets the corresponding status input appropriately.



ANALOG for DIGITAL

Note that AFD points can be placed anywhere in the analog scan, but they must be placed sequentially in a single group. Suggested analog hardware configuration is as follows:

1. MAT - Analog Multiplexed Cards
2. AFD - Analog for Digital Cards (or MAT used as such)
3. CAT - Counter Analog termination cards

Remember that the total analog points specified to the driver include the AFD points. Once the size of the AFD block is specified, the driver will reduce the number of resulting logical analogs by that amount. Also remember that not all of the points in the AFD block have to be used. It is possible to block out more points than is needed. Specifying a smaller amount is done by providing a channel range (rather than just a start point) for parameter 8, the AFD Status address.

Examples:

```
AIN $328 48 16 A1 16 A17 S9 ; block out 16 analogs for use in AFD at S9-24
                            : Usable analogs reduced to 32
AIN $328 22 16 A1 4 A9   S9 ; use only 4 points on analog card (at A9) for status
AIN $328 48 16 A1 16 A17 S9:s12 ; block out 16 AFD, but use only 4 (S9-S12)
```

COUNTER POINTS

The Intel 8253 or 8254 counter/timer chip forms the basis of the generic I/O pulse type inputs. The counter hardware accumulates the pulses so that turbine meters and other quick pulse inputs can be handled by the relatively slow computer. A separate 16 bit (0-64K count) hardware counter is provided for each of the 3 input channels inside each chip.

Because the counter chip uses 16 bit accumulators, SCADAWARE does not have to read the register as often as on some other I/O systems. The chip can accumulate 65K pulses without a roll-over. The counter points are scanned by the driver as part of the normal task scan, which will take place approximately once per second on typical systems. The accumulated amount is added on each pass to a software totalizer stored for each TSP counter channel. The maximum pulses/sec that can be read is therefore related to task processing speed. Assuming a scan rate of once per second (normal for PC systems), the maximum input rate can be 64K per second.

The 825x counter chip increments whenever the input bit is brought to ground. In order to count the next pulse, the input must be allowed to "float" high by disconnecting it completely (through a contact) or by driving it high with a signal (up to 5VDC max). Unamplified turbine meters must be furnished with an amplifier that provides a 5 volt pulse to trigger the counter.

NOTE: The standard DAS-8 counter chip setup assumes that the first counter channel is used in the A/D conversion process. Many boards, including TEST's standard Computer Boards CIO-AD08, do not require the use of this counter, so this channel is made available for use as a field counter input. It may be necessary to modify the board in order to make this input available. TEST's standard configuration is to provide the input for counter 0 on Pin 6 of the DB-37 analog connector. If the board cannot make this input available, then the first counter chip offset must be specified as "1" to tell the software to skip the unused channel.

Other PC bus boards are available that provide single or multiple Intel 8254 counter chips. These boards can be used just as if they resided on multiple DAS-8 boards. The software only requires the specification of the base address and other information as detailed below:

1. Keyword "Counter" First 8254 chip base address in the PC I/O Space address Offset between sequential circuits

2. Number of counter input points (default is 8)Location in the RTU I/O Table (default is 1)

3. Chip offset for first counter port (default is 0)

```
EXAMPLE:
counter $328, 3          ; use default setups at address $328
counter $328, 5,16,1,2 ; use two chips for 5 total inputs
```

ALERT CHANNEL

The ALERT option allows for any TSP channel to be specified as the failure channel. A failure could occur as a result of a hardware failure, or a power supply problem that causes a timeout while waiting for an I/O command to complete. When a failure is detected, the current value of the designated channel will be incremented by 1. Normally, a status or value channel not associated with the actual I/O will be used to receive the alarm alert.

For example, a system with 16 status points could be configured with 17 total TSP status points (at the system level). Channel S17 could then be designated as the alert channel. An error in the driver will cause S17 to become active. The actions taken from this point are the same for any status channel. Horns, blinking displays, and command file execution can all take place when the error occurs.

PHYSICAL INSTALLATION CONSIDERATIONS

The Generic I/O system is a relatively slow speed interface that allows up to 20 feet of ribbon cable to be used between the PC and the farthest termination card. Most RTU systems should not need more than 6' of cable, and longer cables may require shielding to avoid signal interference.

It is important to avoid overloading the analog and counter input channels with voltages higher than 5VDC. In the case of analogs, higher voltages will saturate the multiplexers and cause errors in reading adjacent channels. Counter channels can also be damaged by voltages over 5VDC. TEST's termination boards contain voltage snubbing zener diodes and other devices to reduce damage from overloading. However, inputs should never be connected to damaging voltages.

GIO DRIVER SETUP

The Generic I/O driver program requires setup of a specific DRIVER type task within SCADAWARE. This task will handle scanning of the generic I/O points as described in a specific setup file. The driver task is defined in the DAT file which is processed when SCADAWARE begins execution. As part of the overall system startup, the driver task will be started, causing it to process the setup file and start I/O scanning. More than one driver task can be defined in the DAT file, each handling separate hardware. Each task operates independently.

When defining the driver task, the keyword GENERIC is used to tell SCADAWARE which type of driver task to establish. A file name must be provided on the task definition line telling the system where to locate the setup information when the task is eventually started (or restarted). If a file name is not specified, the default name RTU.GIO is used (for RTU GENERIC I/O data).

Note that this is a multi step process. First, the a GENERIC driver task must be specified in the DAT file. Next, an appropriate text data file must be prepared which contains the setup information for the driver to use when accessing the GIO hardware. Later, after the system is loaded, a TASK START operation must take place to get the driver task into the multi-tasker loop. This is normally done near the end of the TSP procedure called STARTUP.

The information contained in the GIO control file tells the driver how many PC interface board setups are present, their addresses, and other information about the cards connected to each PC interface board. In most cases, default information will be used if not supplied by the user. However, it is always better to completely understand what is going on and provide as much information as possible directly in the file.

Each line in the control file begins with a keyword followed by required and optional parameters. Each keyword provides a specific type of information to the driver, and the driver will build it's internal control tables from the data in this file. Changes in the setup only require simple text editing of this file in order to modify the hardware or software setup of the system. Changes can be made online, but the driver task must be restarted in order for the changes to be used. This is usually done with the command line TASK DRIVER START, although it is possible for the task name to be other than DRIVER, especially when more than one driver is installed on a single system.

The keywords used in the Generic I/O system are:

AIN Setup analog inputs on current group.
Defines an analog input circuit with starting address, point count, etc, as described in the section on analog inputs.

ALERT Identify channel to alert of MB errors.
A channel can be designated to detect I/O driver problems, normally associated with analog circuit failures. If the driver detects a problem, it will set the ALERT channel to 1. Any processing from that point depends on how the Alert channel is programmed by the user.

COUNTER Setup counter inputs on current group
Define a set of counter inputs as defined elsewhere in this document.

DELAY Specify non-standard Analog Multiplexer delay
The system will select a multiplex delay based on suspected CPU speed. The user can override this value by specifying a number between 0 and 4096. Typical values are 3 for a slow 8088 processor, 50 for a medium speed 386, and 100 for a 486 or higher.

FAST Permit per-tick processing of fast status inputs
Status input processing can be done on each system tick, or on each Driver task scan. The default is each task scan. If high speed, short duration status inputs are required, then specifying FAST in the GIO file will set the currently defined Status input group to be scanned on each system tic, approximately every 50 ms.

MIN Minimum analog change value to change corresponding TSP channel
The analog system normally requires at least 1 bit of change in the analog reading in order to bother with informing SCADAWARE that the value has been changed. This eliminates unnecessary processing of analog inputs which "jiggle" between 2 values. The MIN setting permits a higher value to be used. Note that the MIN value is shifted left 3 bits to match the shifting done to convert the 12 bit A/D reading into a SCADAWARE compatible integer. Therefore, the value of 1 is specified as 16, 2 as 32, 3 as 63, etc.

MSG Display any text message during file processing
The driver will output the specified text message to the system console. This is used as a diagnostic tool to track processing of the GIO file and is not normally used.

OUTPUT Setup outputs on the current status group.
Defines a Status Output group as described earlier in this document.

SLOW Turn off FAST status input processing
Overrides the default setting for Fast (per-tick) processing of status inputs. The default selection is based on expected system performance, normally off for 8088 processors, and on for higher speed CPUs.

STATUS Setup status inputs on current group.
Defines a Status Input group as defined earlier in this document.

WAIT Specify wait period for GIO analog settling
During analog conversions, the processor will enter a wait loop while testing for the end of conversion signal from the board. The WAIT parameter determines how many loops the program will make before giving up and signaling an analog failure via the ALERT channel. Typical values automatically selected by the program are 10 for a slow processor, 150 for a 386, and 200 for a high speed 486 or Pentium.

During processing of the GIO file, some keywords apply to the most recently defined PC interface circuit group. Ech I/O point definition starts with a channel type line (Status, AIN, etc) followed by modifier lines (Fast, wait, etc) as necessary. Depending on the keyword, the modifier lines may apply to the entire driver, or only to the most recently defined point group of the appropriate type.

Normally, each point definition keyword creates a separate physical driver circuit in the PC. If, for some reason, two separate (i.e. non-sequential) groups of the same type of circuit are required on the same PC, the driver can be programmed to treat the second group as a separate entity rather than as a sequential unit of the first entry. This is most often used to specify multiple analog input cards that do not use multiplexed terminations, and can therefore only handle 8 input each. If the analog point count was specified as 16, the driver would assume one board with 2 multiplexed terminations. If the actual case is 2 boards, each with 8 non-multiplexed terminations, then the driver must be configured to treat the 16 as 2 separate 8 point boards. Therefore, separate ANALOG definition lines must be used to properly configure the system for only 8 inputs per analog circuit.

SAMPLE GIO CONTROL FILE

The first example is for a single Generic interface card that has mixed multiplexed and non-multiplexed analog inputs. This file is normally named after the RTU location (such as MP209 or HI523) and has a file type of .GIO. Therefore, the complete file name would be MP209.GIO or HI523.GIO.

```
; Simple Generic I/O Setup with one interface board
AIN  $320 22 16 1 ; 2 mpx + 1 mpx
counter $324 3 16 1
Status $328 16 16 1 0 ; first port on first chip
output $328 8 16 1 2 ; port 3 on the first chip
```

The next example is for a system with multiple interface boards analog, status, and counter channels. In this case, the status and counter circuits can be setup with single lines. The analog section, however, requires two separate lines because each line will only define 8 non-multiplexed inputs.

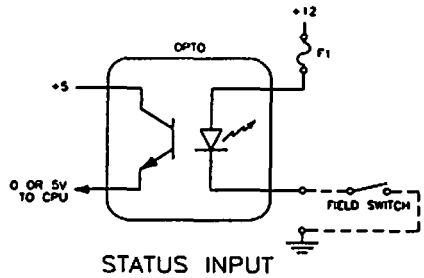
```
; Complex Generic I/O Setup with multiple interface boards
ain   $320 8 16 1 ; one non-MP the analog input
counter $324 6 16 1 ; 3 on each card
status $328 32 16 1 0 ; first port on first chip
FAST          ; insure that per-tick processing takes place
output $338 8 16 1 2 ; port 3 on the second chip

Start the second interface group

ain  $330 8 16 9  ; the next non-mpx analog input card
```

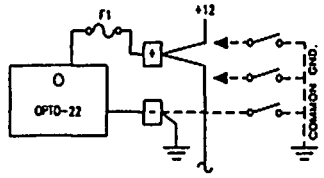
MIO - MULTI I/O STATUS TERMINATION

The Multi I/O interface provides 8 points of optically isolated input or output which connects field inputs and outputs to the Generic I/O parallel interface. This interface accommodates a total of 24 points, in three 8 point groups. Each MIO board handles one group, designated as A, B, or C for each 24 point interface. Each MIO card can be designated as either Input or Output (not both) with an on-board jumper; jumper in for input, out for output.



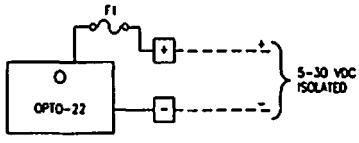
STATUS INPUT

The individual opto modules installed for each point are selected from a variety of Opto-22 standard single point modules. Each input is wired to 2 removable terminal points on the card edge. A pico fuse is also provided for each point for circumstances which require individually fused points. These fuses are often jumped out for status inputs because short circuit protection is normally provided elsewhere in the RTU design. Outputs, however, may use the fuses to prevent overload of each individual point.

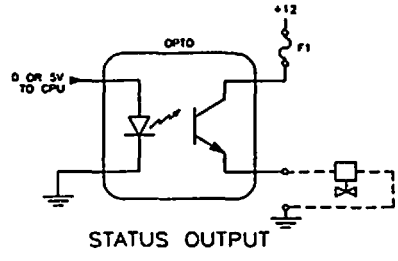


RTU VOLTAGE
MIO TERMINATION

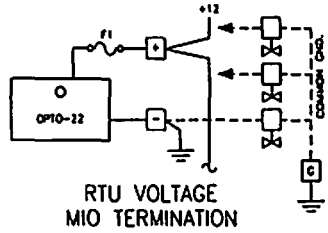
Most RTU applications use a "pull to ground" for status inputs. Closing a field contact to ground completes the circuit, signaling an ON condition to the RTU. Using a grounding input eliminates short circuit problems with field wiring because a shorted field wire turns on the point, but does not blow a fuse. Note that the NEC prohibits the use of grounding switch circuits in cases where the input controls the action of a motor or other load which can cause injury or damage. Therefore, the grounding input system is suitable for monitoring points only, which happen to be the majority of inputs used in a SCADA system.



EXTERNAL VOLTAGE
MIO TERMINATION



STATUS OUTPUT



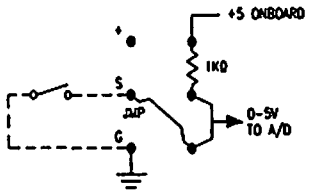
RTU VOLTAGE
MIO TERMINATION

CAT - COUNTER ANALOG TERMINATION

The CAT card provides teremination and scaling resistors for 3 counter (pulse) input points, and 8 non-multiplexed analog inputs. This termination card is the basic unit used in the GIO analog and counter system. If 8 or fewer analogs are required, this card is all that is required. If more than 8 are required, than a mix of Multiplxed (MAT) cards and one CAT card can be used to expand the original 8 GIO inputs up to 64.

A termination circuit is provided for each analog and counter input to scale the input signal to the required 0-5VDC required by the GIO interface. Various combinations of jumpers and resistors can

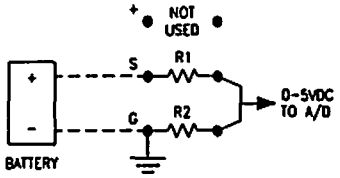
be installed to change 4-20ma into 1-5 volts, or to downscale a battery voltage to the 5 volt maximum allowed by the GIO system.



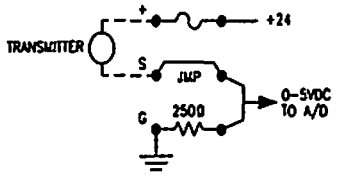
CAT/MAT TERMINATION

MAT MULTIPLEXED ANALOG TERMINATION

SCADAWARE uses the 3 digital signals on the analog ribbon cable to control external multiplex devices on the Multiplexed Analog Termination (MAT) card. Each MAT card takes 8 separate analog inputs and, by use of an on-board mux, passes them on to the computer over the same GIO analog interface point. This multiplexing expands each of the original 8 analog points into 8 new points, providing a net gain of 7 analog channels. The diagram below shows the A/D schematic:



CAT/MAT TERMINATION



CAT/MAT TERMINATION

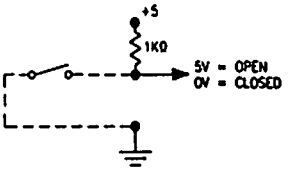
The scaling resistor circuits of the MAT are very similar to those on the CAT card. The MAT has an additional position which can be used to install a zener diode or noise suppression capacitor across each input.

A MAT card jumper must be set to place each card onto one of the 8 original analog lines of the GIO interface. Each card should have only one point jumped.

AFD ANALOG FOR DIGITAL TERMINATION

The AFD 16 point termination card appears to the GIO interface as two separate MAT analog cards. Instead of scaling resistors, the AFD provides built-in high-density opto isolators for all points on the card. The card is ideal for switch input situations where a common power source and ground can be used for all inputs. Each point is provided with a single removable terminal position. The field contact for each point is connected between the terminal point and the common ground. Additional removable terminal points are provided to terminate the common ground wires from the field.

The AFD also contains a linear supply which inputs 10-30 VDC and produces +5 volts to run the AFD circuitry. Therefore, no 5 volt power is required from the analog ribbon cable. The AFD board supply connects via removable terminal points on the edge of the card.



ANALOG for DIGITAL

-End-

TOTAL ENGINEERING SERVICES TEAM, INC.TEST INC.

TEST INC.

OFFICE	MAIN NUMBER	FAX NUMBER
New Orleans, LA	(504) 371-3000	(504) 371-3001
Lafayette, LA	(318) 269-0911	(318) 269-0910
Houston, TX	(713) 467-3113	(713) 467-8113
Ventura, CA	(805) 658-0403	(809) 658-9975
Singapore	65-533-4108	65-534-2403
Bahrain	973-690-575	973-697-010

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